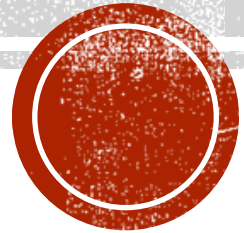
BIPOLAR JUNCTION TRANSISTOR

Unit- II



INTRODUCTION

- Bipolar junction transistor is a three-terminal device.
- Three-terminal devices are far more useful than two-terminal devices(diodes), because they can be used in a multitude of applications, ranging from signal amplification to the design of digital logic and memory circuits.
- The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal.
- It was invented in 1948 at the Bell Telephone Laboratories.
- It enjoyed nearly three decades as the device of choice in the design of both discrete and integrated circuits.
- Currently, it is replaced by Metal oxide semiconductor field effect transistor.
- The BJT remains popular in discrete-circuit design.

DEVICE STRUCTURE

- Figure 1 shows a simplified structure for the BJT.
- Two types
  - NPN
  - PNP
- Semiconductor regions:
  - Emitter region
  - Base region
  - Collector region
- Junctions
  - Emitter–base junction (EBJ)
  - Collector–base junction (CBJ).
- Modes of operation
  - Active mode
  - Cutoff mode
  - Saturation mode.

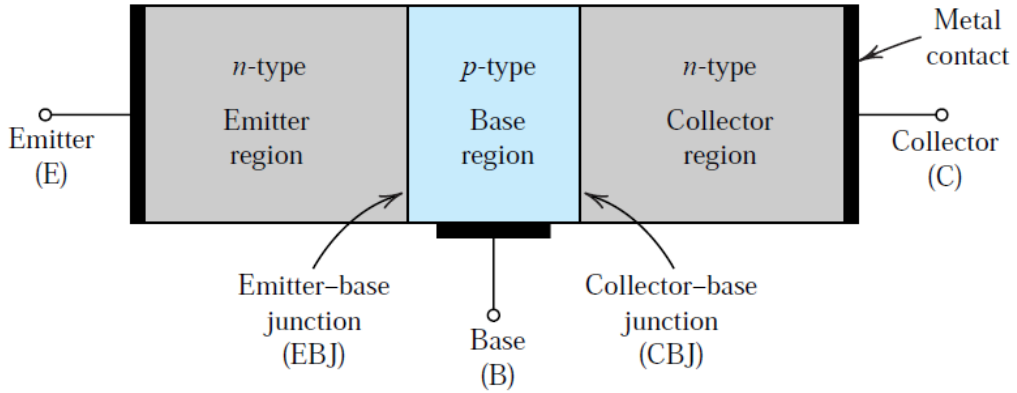


Fig.1: A simplified structure of the *npn* transistor.

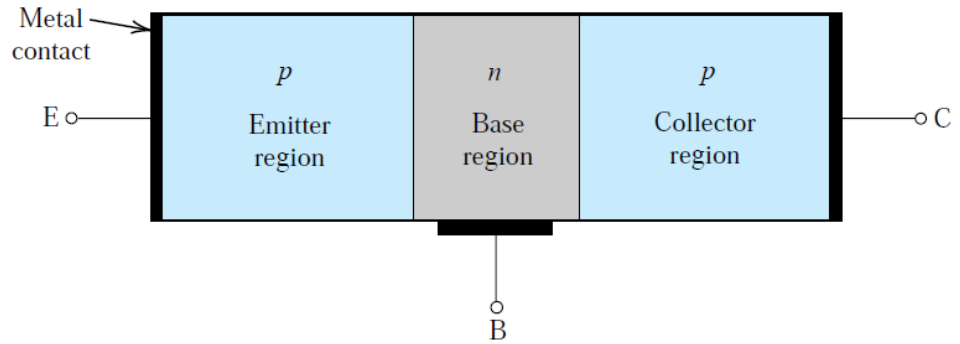


Fig.2: A simplified structure of the *pnp* transistor

Depending upon the bias condition of two junction(EBJ & CBJ),different modes of operation are obtained:

MODES OF OPERATION		
Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

- Active Mode (Forward Active) is the most important mode of operation. In this mode, the BJT operates as an amplifier.
- BJT operates as switch in cut-off & saturation mode.

OPERATION

- Two external voltage sources (shown as batteries) are used to establish the required bias conditions for active-mode operation.
- The voltage V_{BE} causes the *p*-type base to be higher in potential than the *n*-type emitter, thus forward-biasing the emitter–base junction.
- The collector–base voltage V_{CB} causes the *n*-type collector to be at a higher potential than the *p*-type base, thus reverse-biasing the collector–base junction.
- The collector current i_C as

$$i_C = I_S e^{v_{BE}/V_T}$$

$$I_S = A_E q D_n n_{p0} / W$$

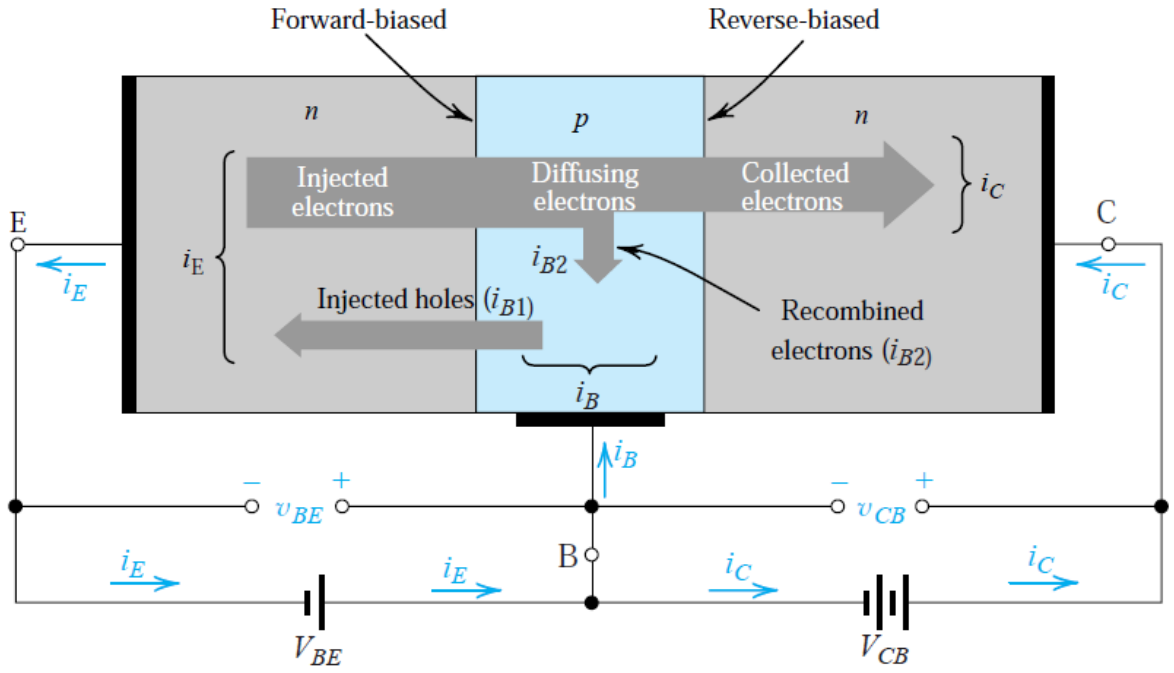


Fig.3:Current flow in an *npn* transistor biased to operate in the active mode

- The base current i_B is composed of two components
  - i_{B1} is due to the holes injected from the base region into the emitter region
  - i_{B2}, is due to holes that have to be supplied by the external circuit in order to replace the holes lost from the base through the recombination process.
- Thus the total base current,

$$i_B = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

Where, β is called the common-emitter current gain

- The emitter current i_E is equal to the sum of the collector current i_C and the base current i_B.

$$i_E = (I_S/\alpha)\, e^{v_{BE}/V_T}$$

$$\alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha}$$

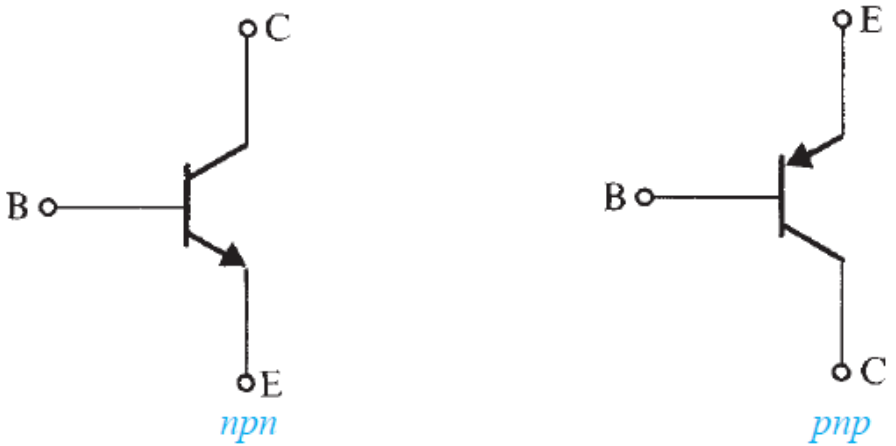


Fig.4:Circuit symbols for BJTs.

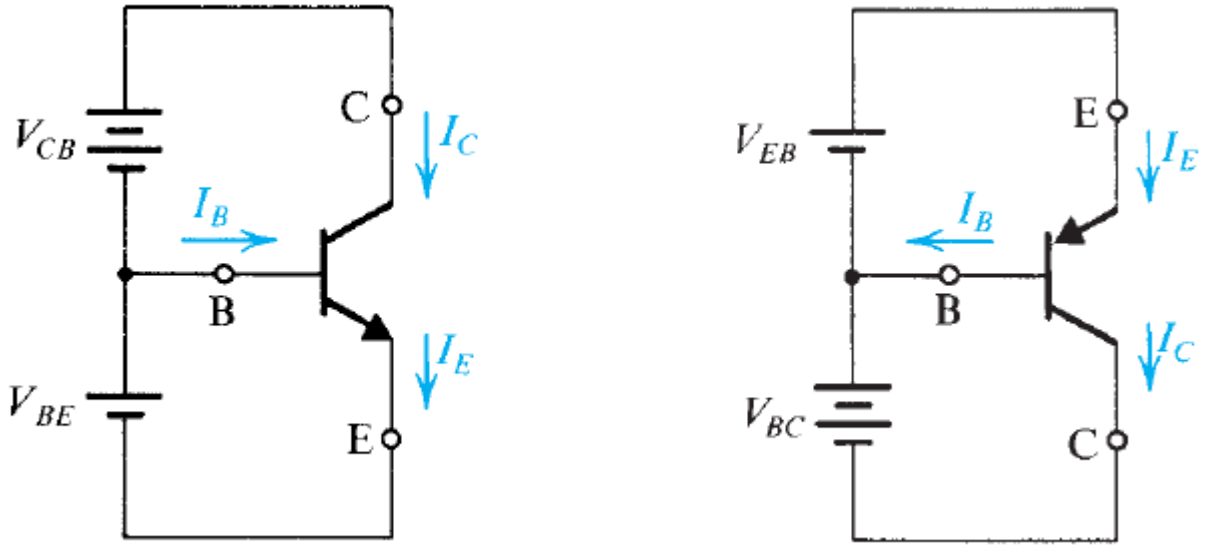


Fig.5: Voltage polarities and current flow in transistors biased in the active mode.

EXAMPLE

Q.1 The transistor in the circuit of Fig. 6 has β = 100 and exhibits a v_{BE} of 0.7 V at i_C = 1 mA. Design the circuit so that a current of 2 mA flows through the collector and a voltage of +5 V appears at the collector.

Solution:

$$R_C = \frac{10\text{ V}}{2\text{ mA}} = 5\text{ k}\Omega$$

$$V_{BE} = 0.7 + V_T \ln\left(\frac{2}{1}\right) = 0.717\text{ V}$$

$$V_E = -0.717\text{ V}$$

$$I_E = \frac{I_C}{\alpha} = \frac{2}{0.99} = 2.02\text{ mA}$$

$$R_E = \frac{V_E - (-15)}{I_E} = \frac{-0.717 + 15}{2.02} = 7.07\text{ k}\Omega$$

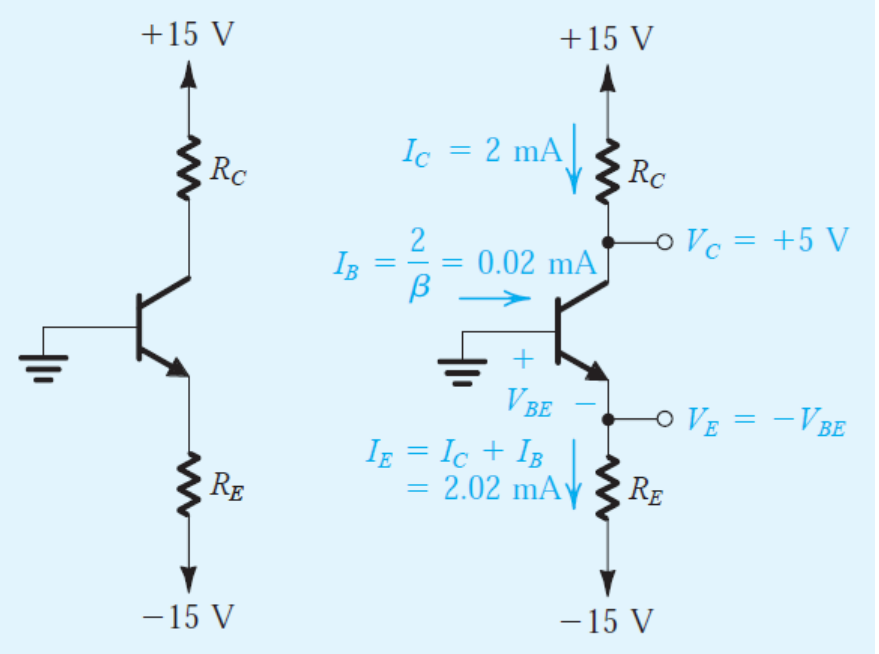
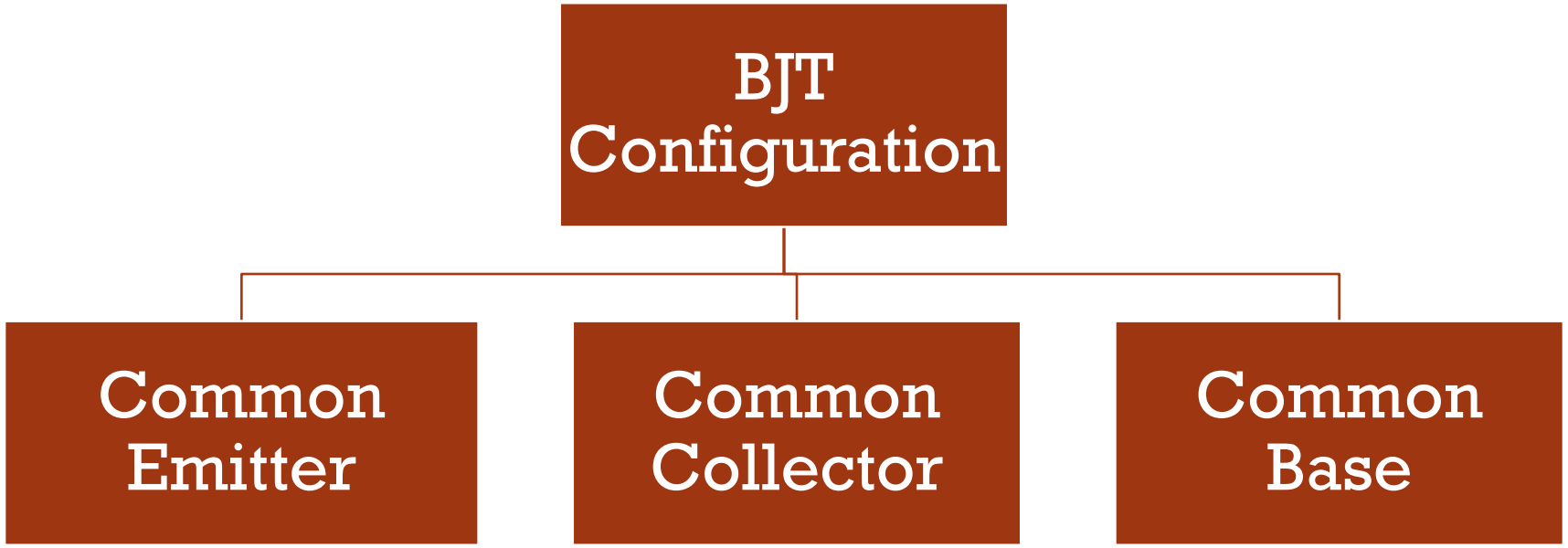


Fig.6:Circuit symbols for BJTs.


BJT Configuration
Common Emitter
Common Collector
Common Base

COMMON EMITTER CONFIGURATION

- The most frequently encountered transistor configuration.
- It is called the common-emitter configuration because the emitter is common to both the input and output terminals.
- Two sets of characteristics are necessary to describe fully the behavior of the common-emitter configuration.
  - Input Characteristics
  - Output Characteristics

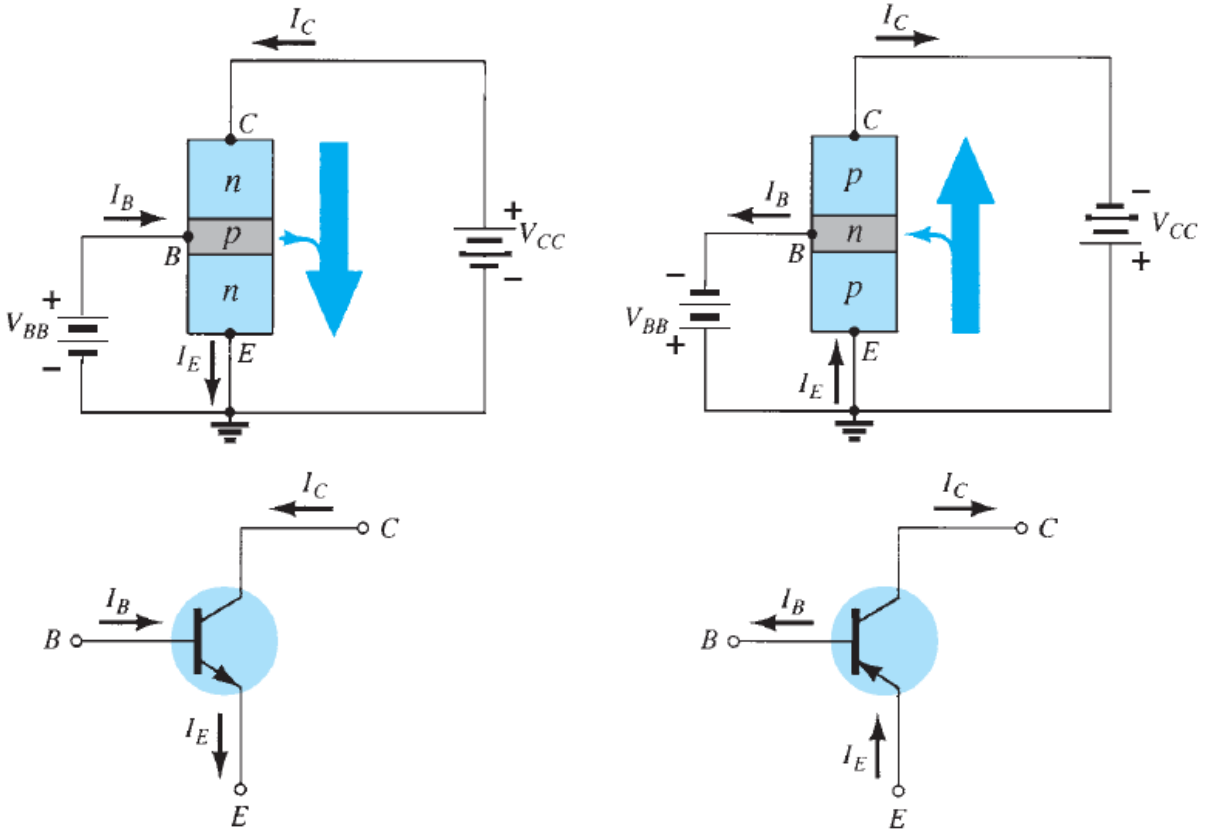


Fig.7(a): NPN Transistor

Fig.7(b): PNP Transistor

Fig.7: Notation and symbols used with the common-emitter configuration

INPUT-OUTPUT CHARACTERISTICS

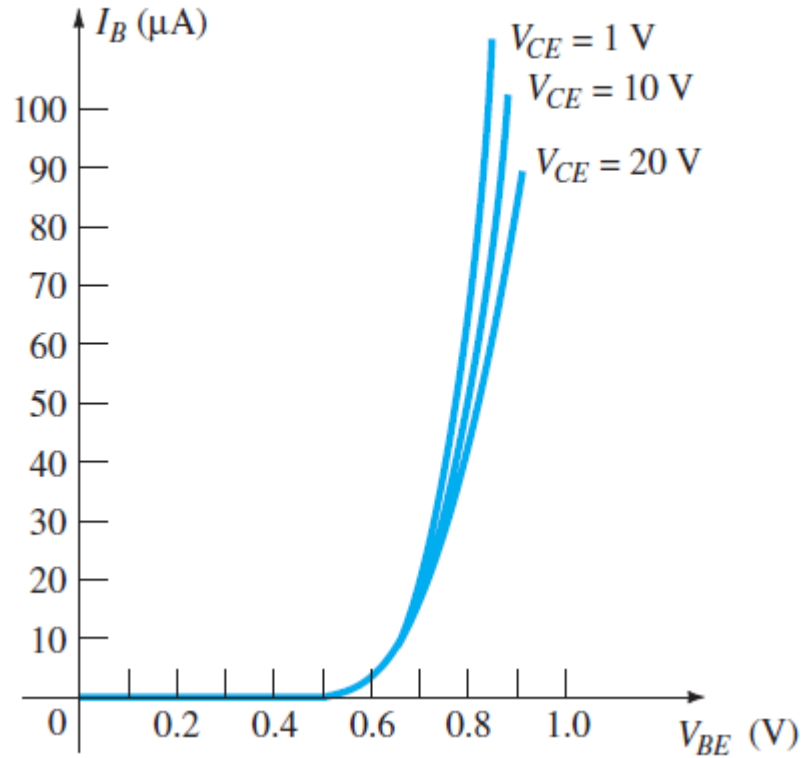


Fig.8(a): Input Characteristics

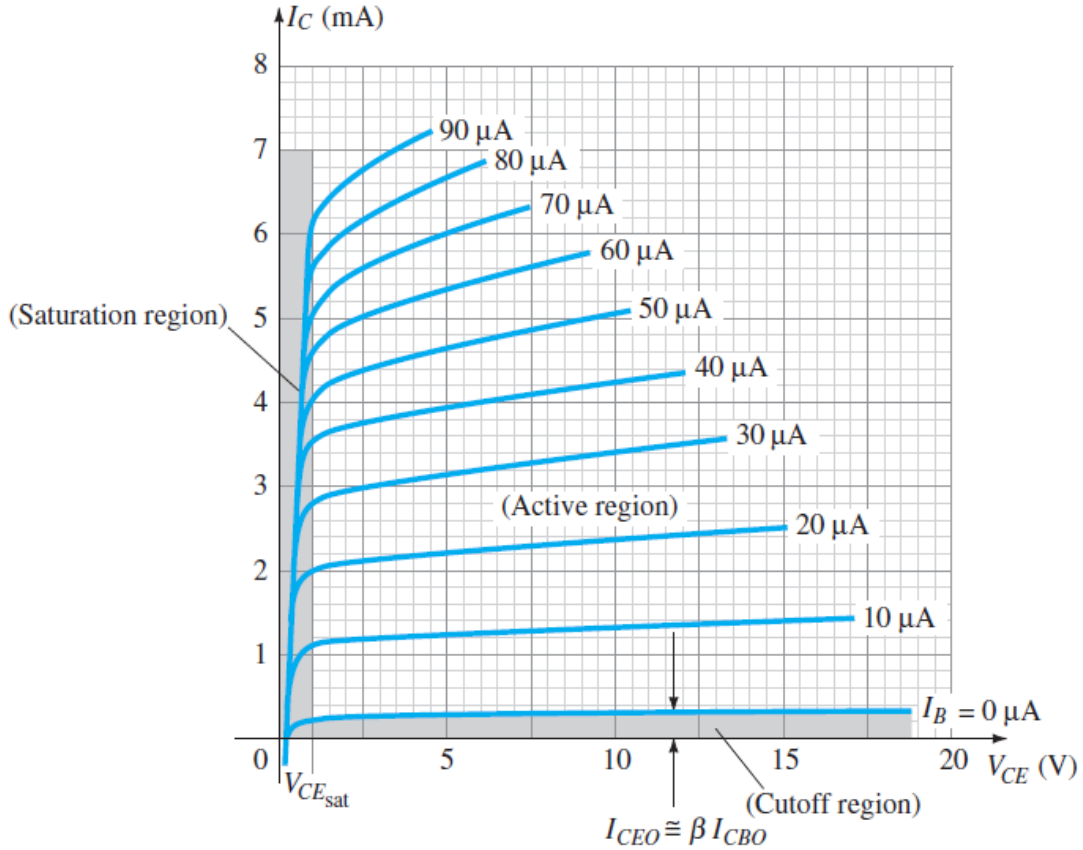


Fig.8(b): Output Characteristics

Fig.8: Characteristics of a silicon transistor in the common-emitter configuration

EXAMPLE

Q.2 To determine all node voltages and branch currents, for the circuit shown in fig. 9. Assume β = 100).

Solution:

$$V_E = 4 - V_{BE} \simeq 4 - 0.7 = 3.3 \text{ V}$$

$$I_E = \frac{V_E - 0}{R_E} = \frac{3.3}{3.3} = 1 \text{ mA}$$

$$I_C = \alpha I_E$$

$$\alpha = \frac{\beta}{\beta + 1} = \frac{100}{101} \simeq 0.99$$

$$I_C = 0.99 \times 1 = 0.99 \text{ mA}$$

$$V_C = 10 - I_C R_C = 10 - 0.99 \times 4.7 \simeq +5.3 \text{ V}$$

$$I_B = \frac{I_E}{\beta + 1} = \frac{1}{101} \simeq 0.01 \text{ mA}$$

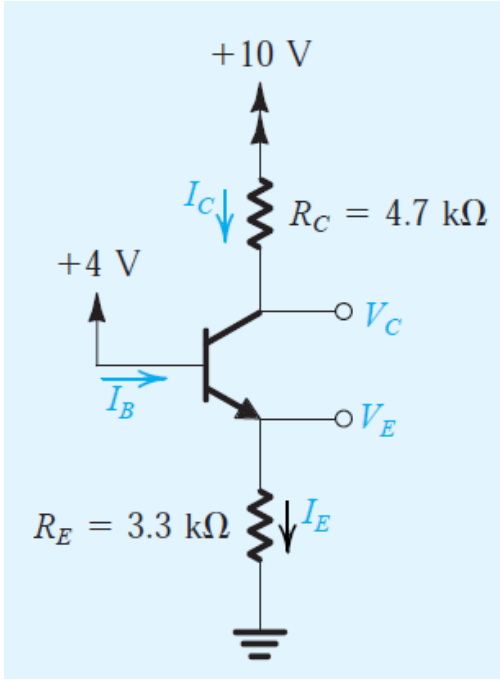
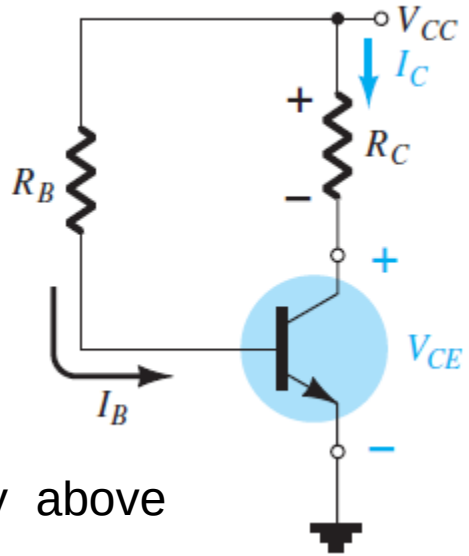


Fig.9

DC LOAD-LINE

$$V_{CE} = V_{CC}|_{I_C=0\,\text{mA}}$$

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0\,\text{V}}$$



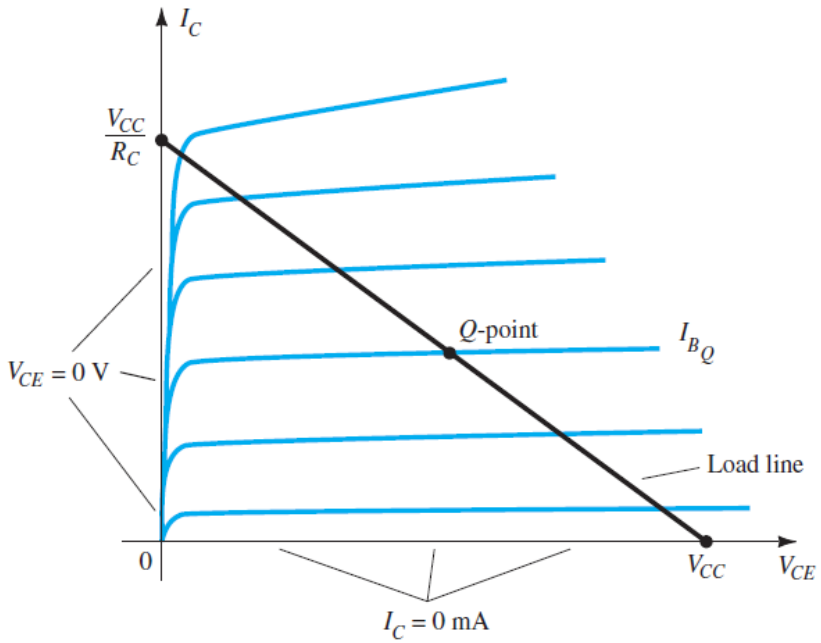


Fig.10: DC load-line Analysis

- By joining the two points defined by above equations, a straight line can be drawn.
- The resulting line on the graph of Fig. 10 is called the *load line.*
- It is defined by the load resistor R_C.
- By solving for the resulting level of I_B, Q -point can be established as shown in Fig.10.

- If the level of I_B is changed by varying the value of R_B , the Q -point moves up or down the load line as shown in Fig. 11(a).
- If V_{CC} is held fixed and R_C increased, the load line will shift as shown in Fig. 11(b).
- If R_C is fixed and V_{CC} decreased, the load line shifts as shown in Fig. 11(c) .

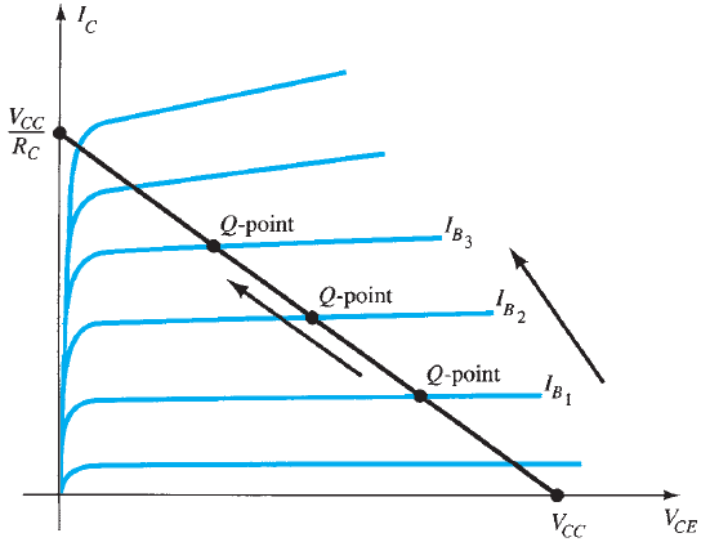


Fig.11(a):Movement of the Q-point with increasing level of I_B

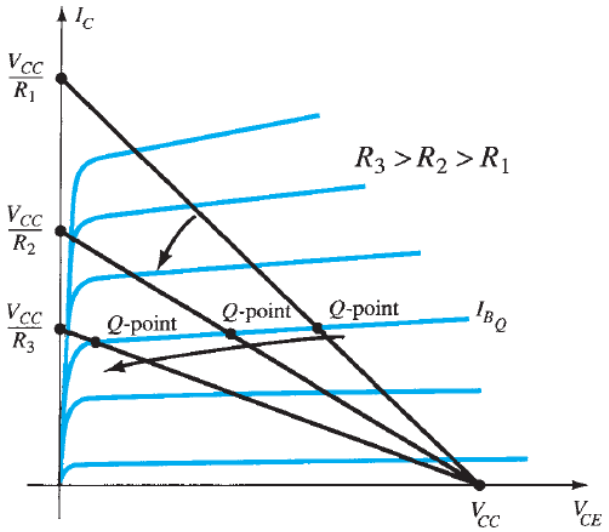


Fig.11(b): Movement of the Q-point with increasing level of R_C

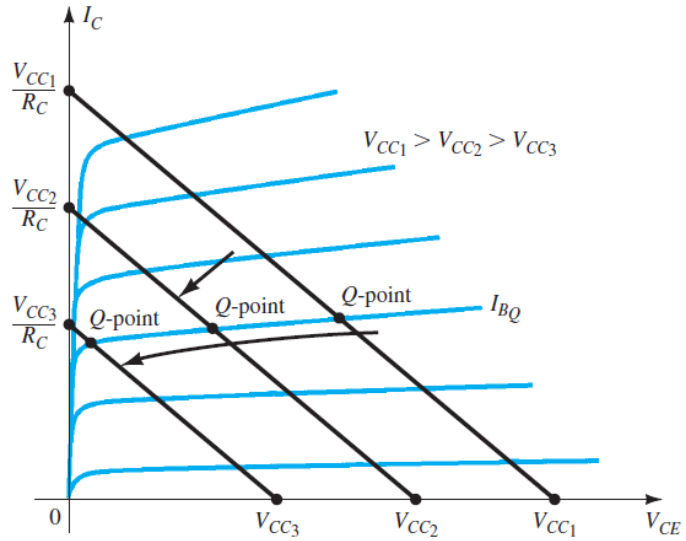


Fig.11(c):Effect of lower values of V_{CC} on the load line and the Q-point.

DC BIASING

- The analysis or design of a transistor amplifier requires a knowledge of both the dc and the ac response of the system.
- Biasing refers to the application of dc voltages to establish a fixed level of current and voltage.
- For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.
- Operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q -point).
- For the BJT to be biased in its linear or active operating region the following must be true:
  - The base–emitter junction must be forward-biased (p-region voltage more positive), with a resulting forward-bias voltage of about 0.6 V to 0.7 V.
  - The base–collector junction must be reverse-biased (n-region more positive), with the reverse-bias voltage being any value within the maximum limits of the device.
- Different biasing circuit used to bias BJT are:
  - Fixed-bias Configuration
  - Emitter-bias Configuration
  - Voltage Divider Bias

FIXED BIAS CONFIGURATION

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

$$V_{BE} = V_B - V_E$$

$$V_{BE} = V_B$$

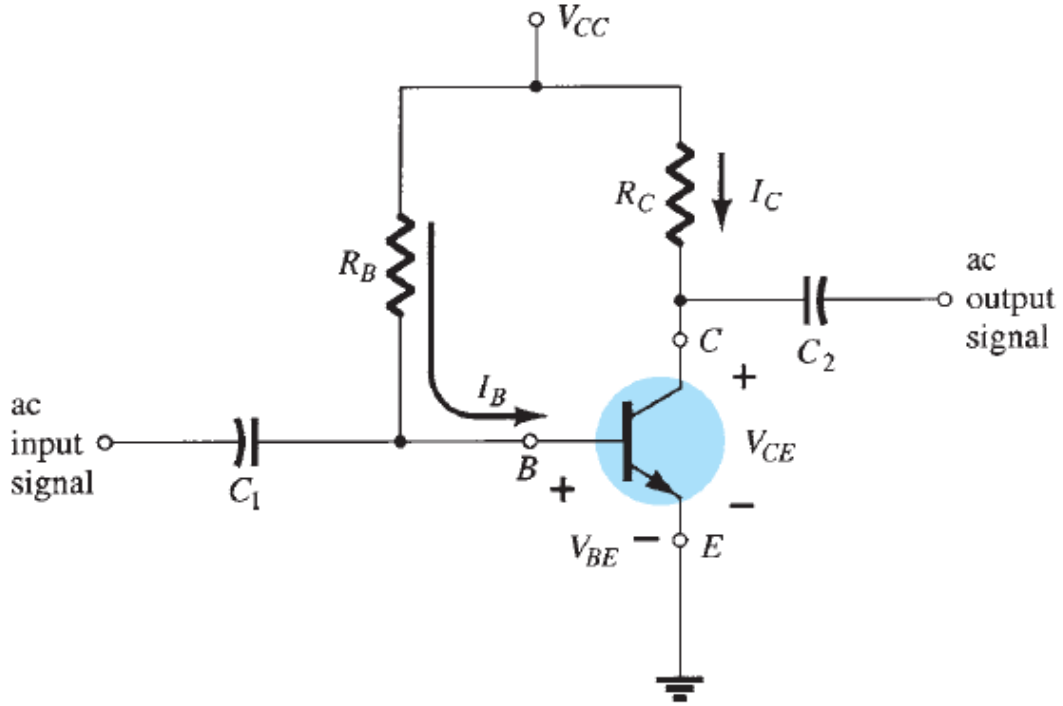


Fig.11: Fixed-Bias Circuit

EMITTER BIAS CONFIGURATION

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$R_i = (\beta + 1)R_E$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E$$

$$V_C = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_B R_B$$

$$V_B = V_{BE} + V_E$$

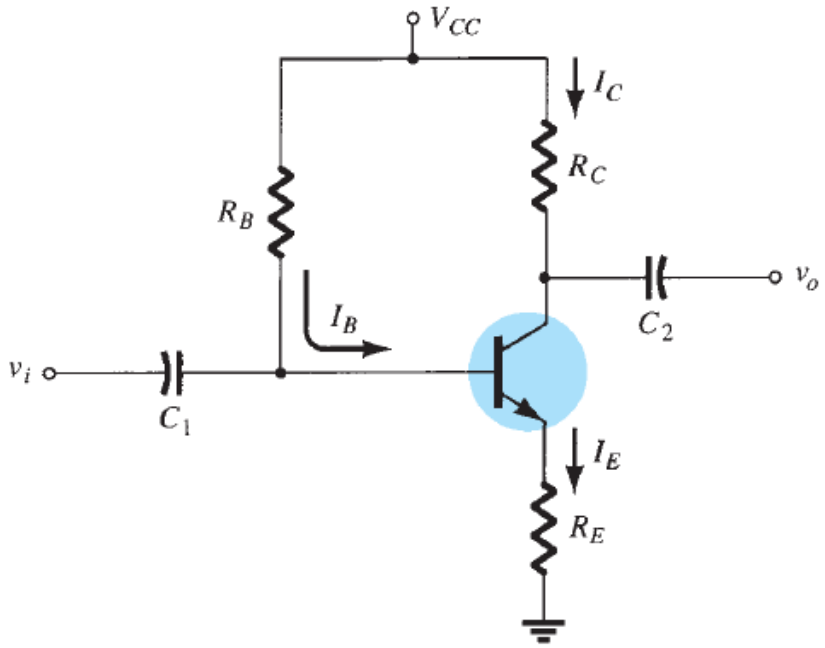


Fig.12:BJT bias circuit with emitter resistor

VOLTAGE-DIVIDER BIAS CONFIGURATION

$$R_{Th} = R_1 \| R_2$$

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

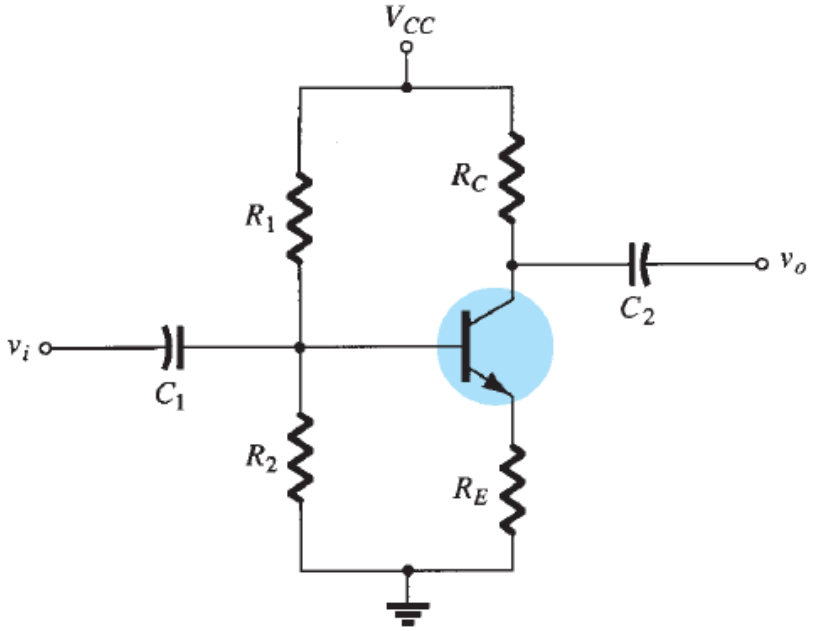


Fig.13:Voltage-divider bias configuration

EXAMPLE

Question: Determine the dc bias voltage V_{CE} and the current I_C for the voltage divider configuration of Fig. 14.

Solution:

$$R_{Th} = R_1 \| R_2$$
$$= \frac{(39\,k\Omega)(3.9\,k\Omega)}{39\,k\Omega + 3.9\,k\Omega} = 3.55\,k\Omega$$
$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$
$$= \frac{(3.9\,k\Omega)(22\,V)}{39\,k\Omega + 3.9\,k\Omega} = 2\,V$$
$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$
$$= \frac{2\,V - 0.7\,V}{3.55\,k\Omega + (101)(1.5\,k\Omega)} = \frac{1.3\,V}{3.55\,k\Omega + 151.5\,k\Omega}$$
$$= 8.38\,\mu A$$
$$I_C = \beta I_B$$
$$= (100)(8.38\,\mu A)$$
$$= \mathbf{0.84\,mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 22\,V - (0.84\,mA)(10\,k\Omega + 1.5\,k\Omega)$$
$$= 22\,V - 9.66\,V$$
$$= \mathbf{12.34\,V}$$

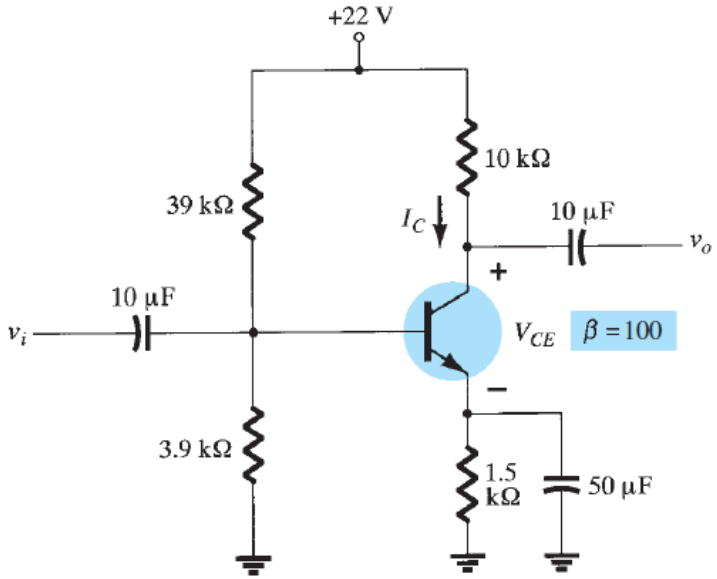


Fig.14

EXAMPLE

Question: For the emitter-bias network of Fig.15 , determine:

a. I_B

b. I_C

c. V_{CE}

d. V_C

e. V_E

f. V_B

g. V_{BC}

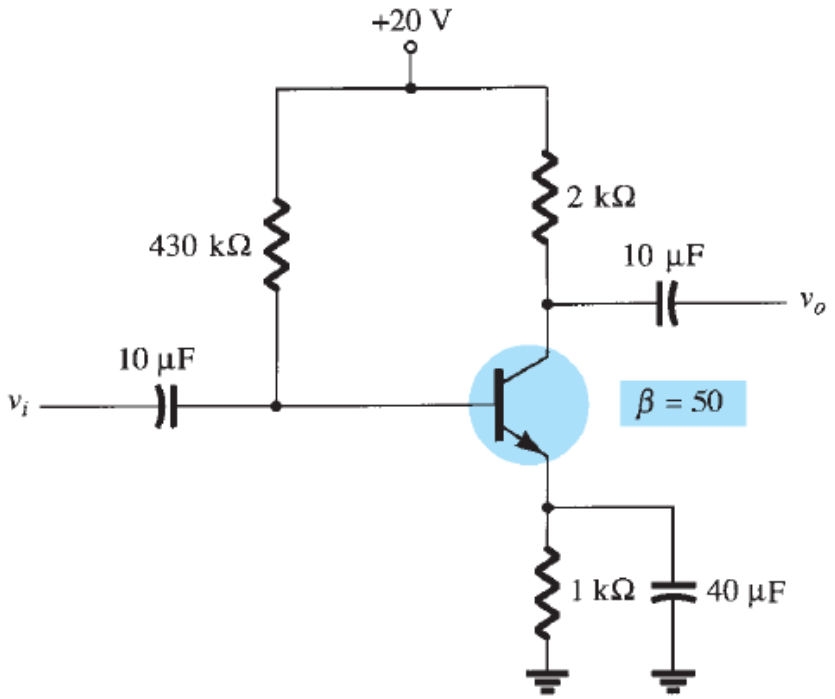


Fig.15

Solution:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$

$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

$$I_C = \beta I_B$$

$$= (50)(40.1\ \mu\text{A})$$

$$\cong \mathbf{2.01\ mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$$

$$= \mathbf{13.97\ V}$$

$$V_C = V_{CC} - I_C R_C$$

$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$$

$$= \mathbf{15.98\ V}$$

$$V_E = V_C - V_{CE}$$

$$= 15.98\text{ V} - 13.97\text{ V}$$

$$= \mathbf{2.01\ V}$$

$$V_B = V_{BE} + V_E$$

$$= 0.7\text{ V} + 2.01\text{ V}$$

$$= \mathbf{2.71\ V}$$

$$V_{BC} = V_B - V_C$$

$$= 2.71\text{ V} - 15.98\text{ V}$$

$$= \mathbf{-13.27\ V}\text{ (reverse-biased as required)}$$

EXAMPLE

Question: Given the load line of Fig.16 and the defined Q -point, determine the required values of V_{CC} , R_C , and R_B for a fixed-bias configuration.

Solution:

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0\ \text{mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\ \text{V}$$

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{10\ \text{mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\ \text{V} - 0.7\ \text{V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

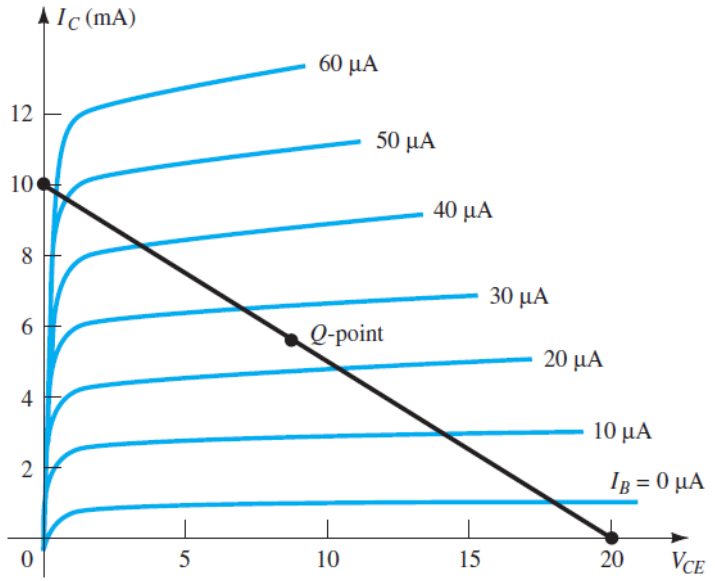


Fig. 16

EXAMPLE

Question: Determine the following for the fixed-bias configuration of Fig.17 .

a. I_{BQ} and I_{CQ}

b. V_{CEQ}

c. V_B and V_C

d. V_{BC}

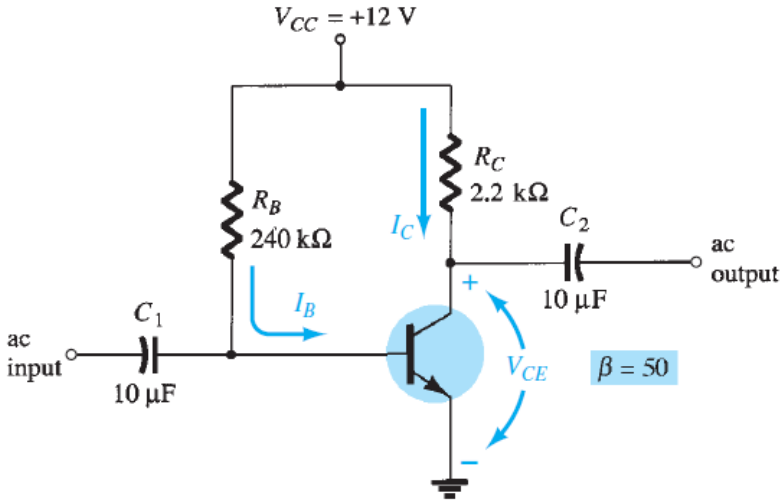


Fig. 16

Solution:

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

$$I_{C_Q} = \beta I_{BQ} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\ V}$$

$$V_B = V_{BE} = \mathbf{0.7\ V}$$
$$V_C = V_{CE} = \mathbf{6.83\ V}$$

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\ V}$$