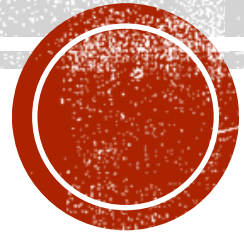
Unit- II

# MOSFET



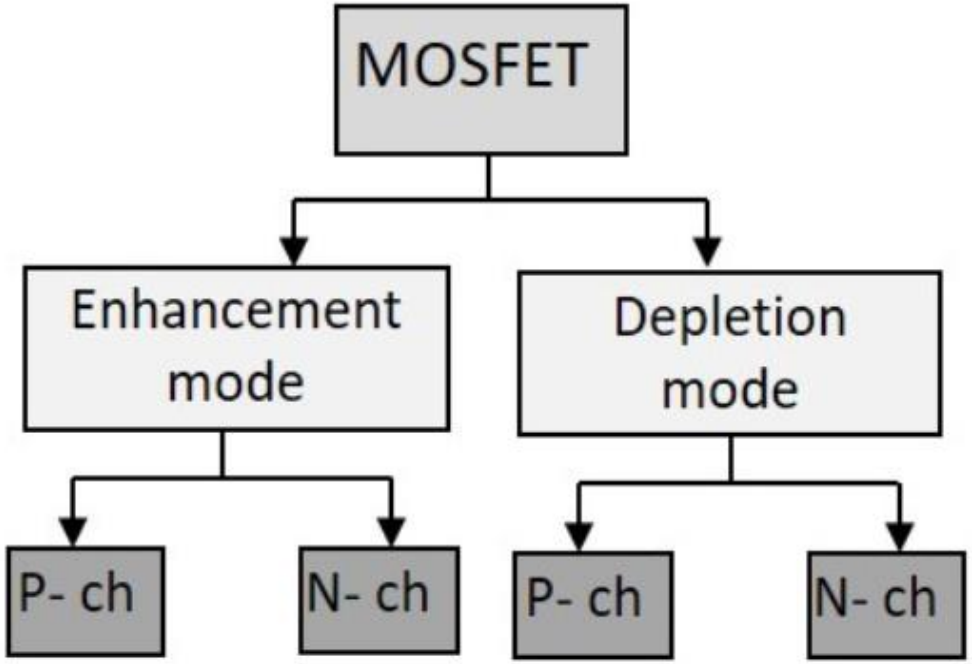
# TOPIC COVERED

- **INTRODUCTION TO MOSFET**
- **ENHANCEMENT MOSFET,**
  - **CONSTRUCTION**
  - **OPERATION AND CHARACTERISTICS**
  - **CURRENT EQUATION**

# INTRODUCTION

- Metal-oxide semiconductor field-effect transistor (MOSFET) is a four terminal semiconductor device
- Mainly used in design of integrated circuits (ICs)
- Compared to BJTs, MOSFETs
  - require very small area on the silicon IC chip
  - Involves simpler manufacturing process
  - Consumes low power.
- Its unique properties have led to the revolution of the semiconductor industry.

# CLASSIFICATION OF MOSFETS




- P- ch = P- channel
- N- ch = N- channel

# ENHANCEMENT-TYPE MOSFET

- The enhancement-type MOSFET is the most widely used field-effect transistor
- It is a voltage controlled device which comes with four terminals named the gate (G), the source (S), the drain (D), and the substrate or body (SS/B).
- The voltage at the gate terminal controls the current between drain and source.

# CONSTRUCTION (N-CHANNEL)

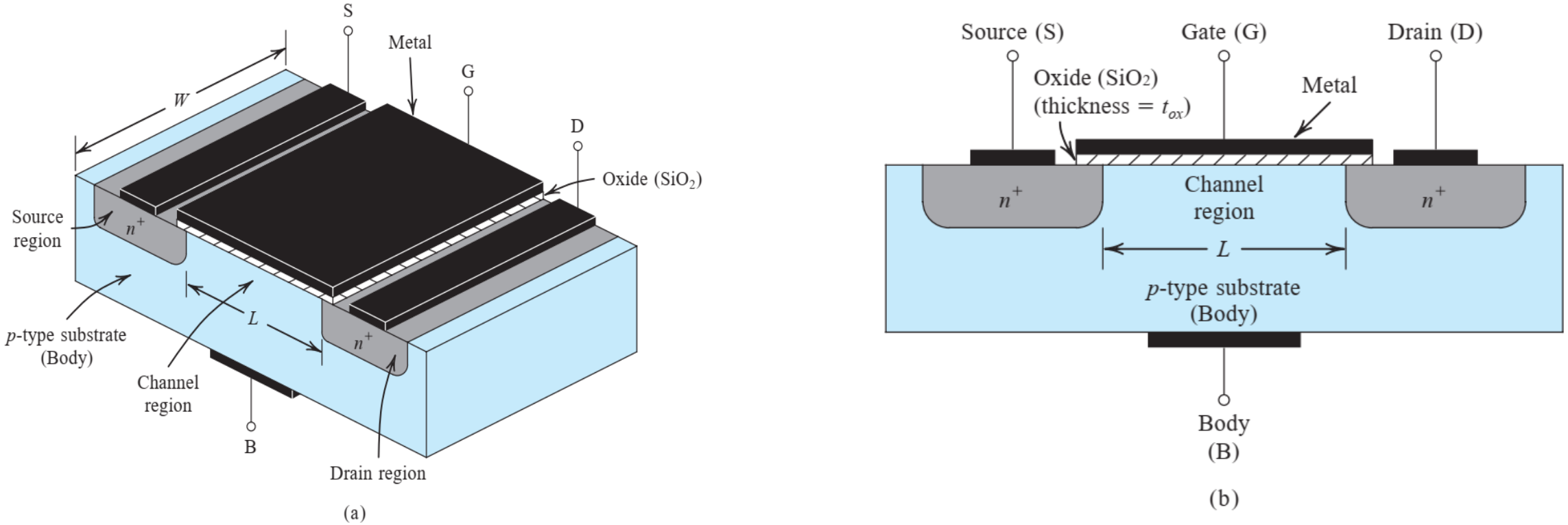
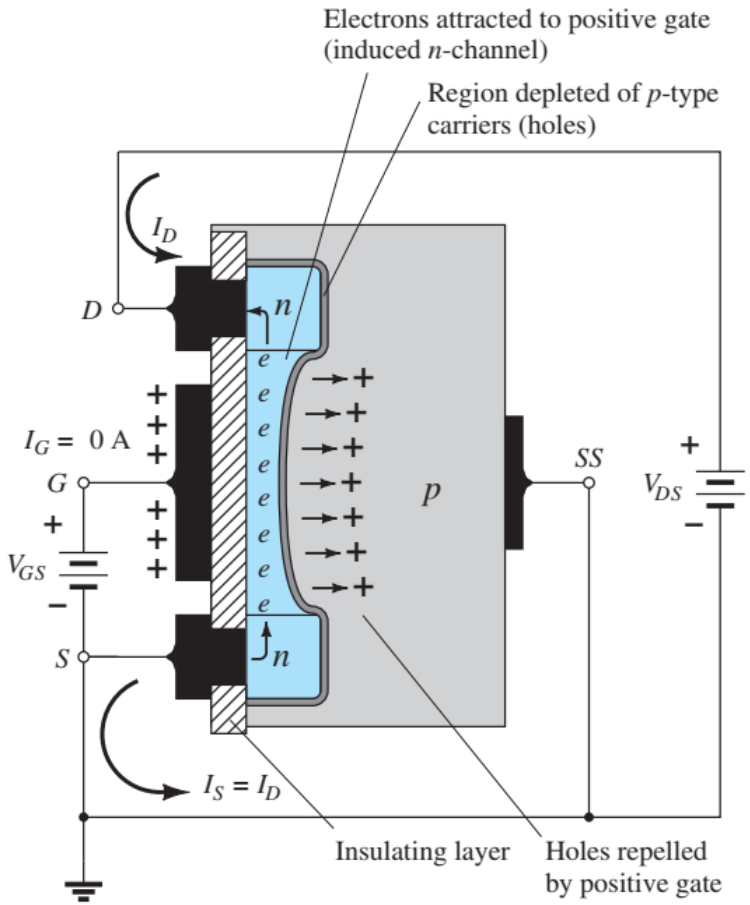



Fig.2 (a) Structure of n-Channel Enhancement MOSFET (b) side view

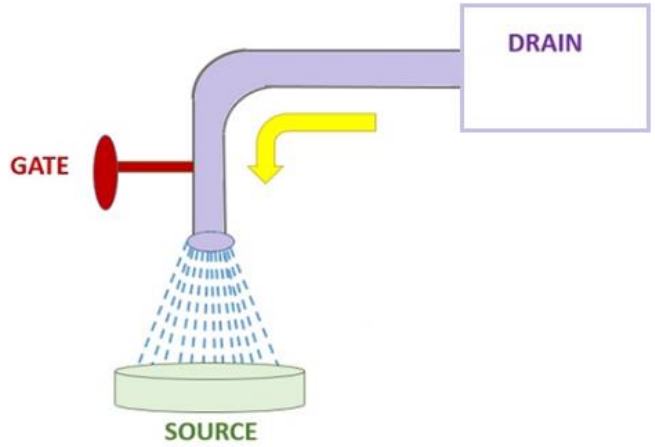
# CONSTRUCTION

- The transistor is fabricated on a p-type substrate, known as body.
- Two heavily doped n-type regions **n+ source** and the **n+ drain** regions, are diffused in the substrate.
- A thin $SiO_2$ layer (that works as insulator) is grown on the surface of the substrate, covering the area between the source and drain regions.
- Metal is deposited on top of the oxide layer to form the gate electrode of the device. Similar metal contacts are also made to the source region, the drain region, and the substrate
- The region between source and drain is known as **channel** region. However, in enhancement type MOSFET channel is not physically constructed during manufacturing.
- Since the gate electrode is electrically insulated from the body (by the oxide layer), MOSFET is also known as **insulated-gate FET** or **IGFET.**

# DEVICE OPERATION




Creating a channel for current flow. A positive voltage is applied to the gate with drain, source and body at ground




Understanding MOSFET through water analogy

The flow of water is analogous to the flow of current from drain to source. The “gate,” through an applied signal (potential), controls the flow of water (current) from “drain” to the “source.”

# CONTINUED..

- With $V_{GS}$ =0 V and $V_{DS}$ >0 , there is absence of a channel, which result in a no drain current.

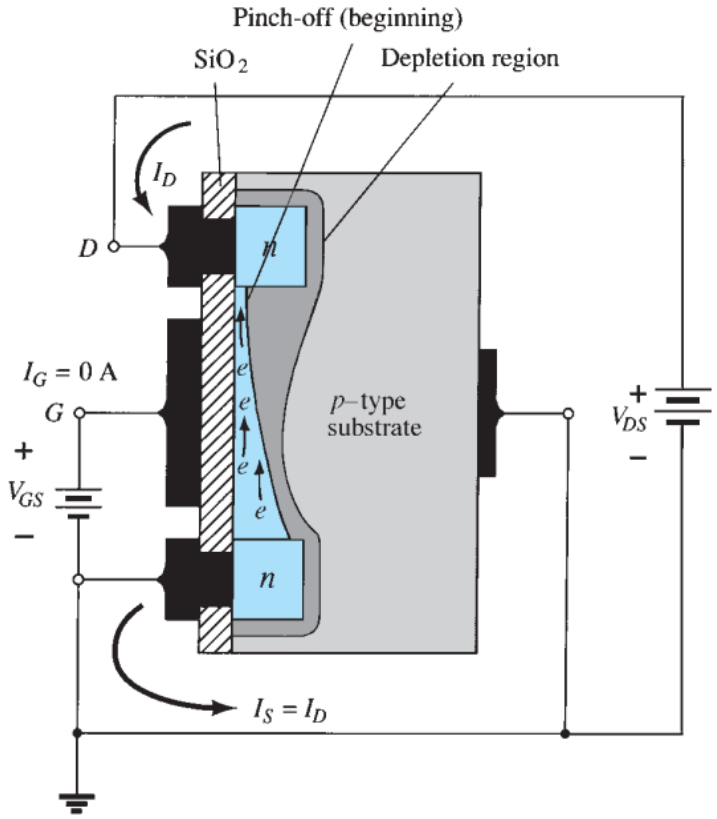
*-This is analogous to the situation, when tap is closed (VGS=0). No matter how much is the water in the drain, no water will come into the source.*

- With $V_{GS}$ > 0 V and $V_{DS}$ > 0 V , Creation of channel and flow of drain current
  - Holes are repelled & Electrons are attracted from the n+ source and drain regions to form a channel in the substrate region near the gate
  - The value of $V_{GS}$ at which a sufficient number of electrons accumulate in the channel region to form a conducting channel is called the threshold voltage and is denoted by $V_{th}$.
  - As $V_{GS}$ is increased beyond the threshold level, channel is enhanced (**hence the name enhancement mode)** i.e. the density of free carriers in the induced channel increases, resulting in an increased level of drain current.

*- This is analogous to the situation, when there is water in tank (positive VDS) and we start opening the tap (VGS ≥ Vth) then water will come out and flow of water will increase if we open the tap by larger extent.*

# CONTINUED..

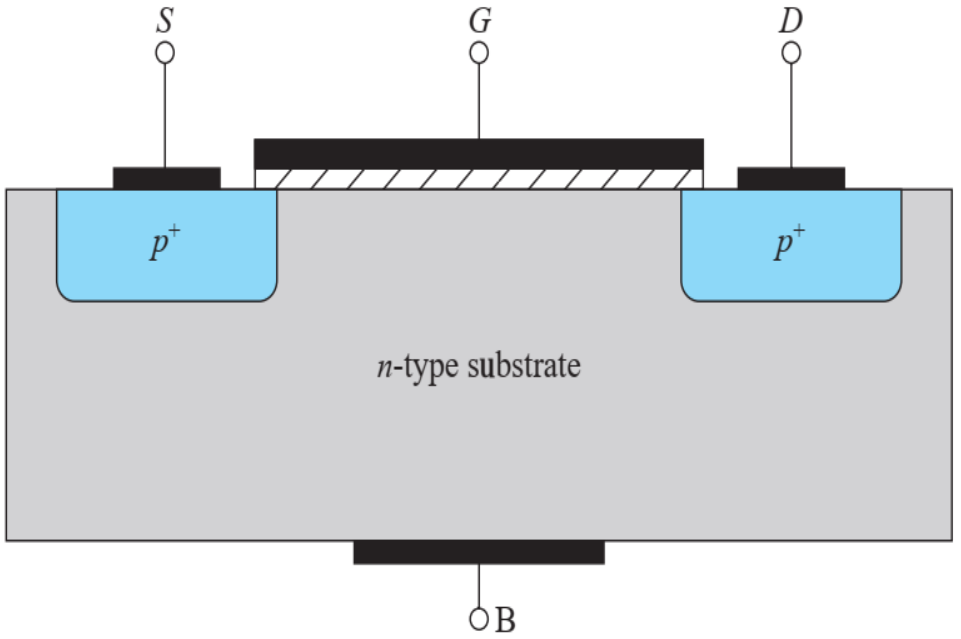
- $V_{GS}$ is fixed at a voltage above $V_{th}$ and $V_{DS}$ is further increased
  - As $V_{DS}$ is increased, the channel becomes more tapered and eventually, the channel will be reduced to the point of pinch-off. The MOSFET is then said to have entered the **saturation region.** The drain current ideally saturates and becomes independent of $V_{DS}$.
  - The voltage $V_{DS}$ at which saturation occurs is denoted by $V_{DSsat}$ given by $V_{GS} - V_{th}$




Operation of the enhancement NMOS transistor as $V_{DS}$ is increased. The induced channel acquires a tapered shape.

# P-CHANNEL ENHANCEMENT MOSFET:

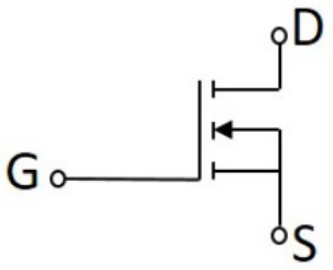
- The structure is similar to that of the NMOS device except that here the substrate is *n* type and the source and the drain regions are *p*+ type

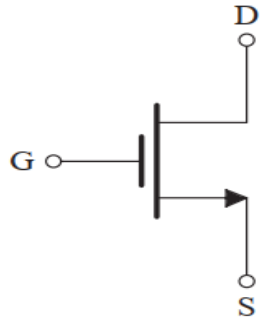



Device structure of p-channel enhancement MOSFET

# DEVICE SYMBOL

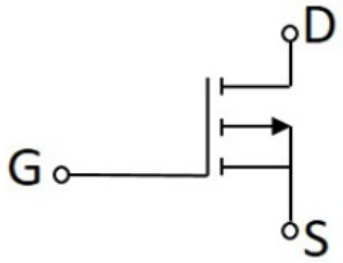
- N-channel enhancement MOSFET (NMOS)

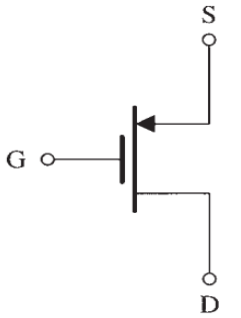



Simplified symbol , B and S are connected

- P-channel enhancement MOSFET (PMOS)




Simplified symbol , B and S are connected

# REGION OF OPERATION AND CHARACTERISTICS

- There are three regions of operation:

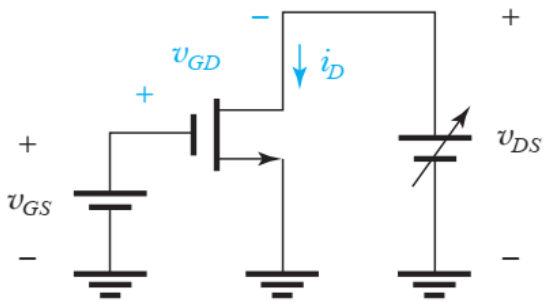
- Cut-off: $\mathbf{V_{GS} < V_{th}}$, no channel is created, the drain current ($I_D$) is zero
- Triode region: $\mathbf{V_{GS} \geq V_{th}}$, Channel is induced, $\mathbf{I}_D$ starts flowing, varies almost linearly with $V_{DS}$ till $V_{DSsat.}$
- Saturation region: $\mathbf{V_{GS} \geq V_{th}}$ and $\mathbf{V_{DS} \geq V_{DSsat}}$, $\boldsymbol{I}_D$ saturates.

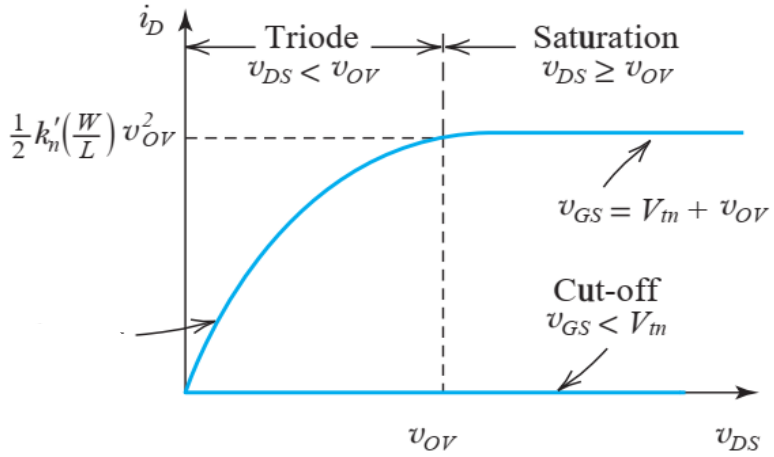
# CURRENT VOLTAGE RELATION

- The conditions and current equations in various regions of operation for the Enhancement N-type MOSFET is summarised on next slide.
  - $V_{tn}$ denotes the threshold voltage ($V_{th}$) of NMOS transistor.
  - $K_n$' is the process transconductance parameter of NMOS.

    $k'_n = \mu_n C_{ox}$ (In amperes per volt squared ($A/V^2$))
  - $V_{OV}$ is overdrive voltage given by

    $V_{OV} = V_{GS} - V_{tn}$




- $v_{GS} < V_{tn}$: no channel; transistor in cut-off; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

### *Triode Region*

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

### *Saturation Region*

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

Then

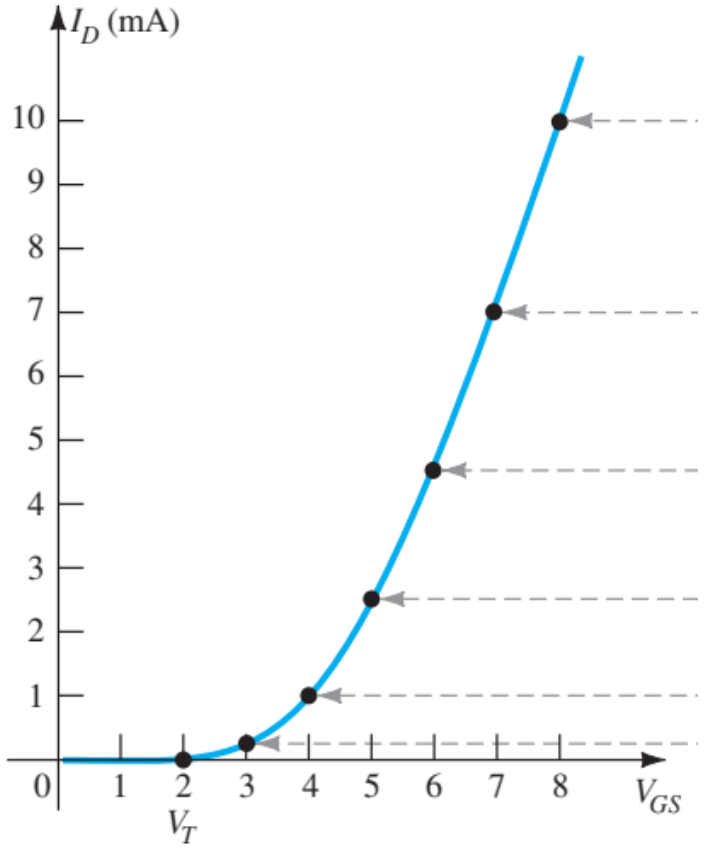
$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

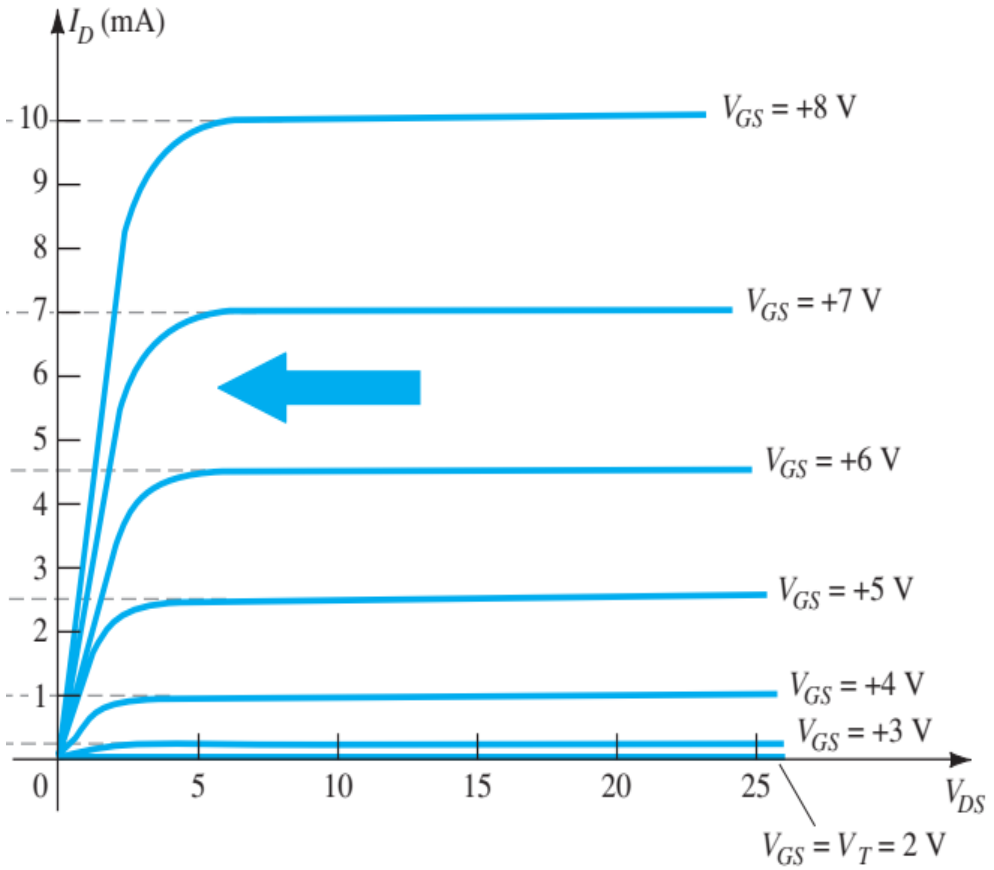
$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

# I-V CHARACTERISTIC FOR N-TYPE MOSFET

**$I_D$-$V_{GS}$ curve**




**$I_D$-$V_{DS}$ curve**



# SOLVED PROBLEMS

Separate Solved Problem Sheet Provided

# REFERENCE MATERIAL FOR FURTHER STUDY

| Sr. No. | Item | Source | Description/link |
|---|---|---|---|
| 1 | Theory | YouTube (Recommended) | https://www.youtube.com/watch?v=l9LBIy9Iox0 |
| 2 | | NPTEL | https://www.youtube.com/watch?v=MuBiC9yz2fc |
| 3 | | Boylestead Book (11th Ed.) | Section 6.8 |
| 4 | Problems for practice | Sedra Smith Book (6th Ed.) | Solved problem: 5.1, 5.5, 5.6<br>Exercise: 5.11, 5.12<br>Problems: 5.18, 5.19, 5.45, 5.46, 5.48<br>Separate Solved Problem Sheet Provided |